

a plurality of bonding areas to where a plurality of bumps of a chip elements are simultaneously jointed by ultrasonic bonding; and

*B3
B.3
bond.*
at least two grooves located proximate to one of said bonding areas to put the bonding area therebetween, at least a part of said grooves extending a certain direction.

14. A circuit board as claimed in claim 13, wherein said conductive layer at said groove is removed.

15. A circuit board as claimed in claim 13, wherein said conductive layer at said groove is thinned --

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 7, 9, and 13-15 are presently active in this case, Claims 7 and 9 having been amended, Claims 13-15 having been added, and Claims 4-6, 8, and 10-12 having been canceled by way of the present Amendment.

The Applicants wish to thank Examiner Kamand Cuneo for the courtesies extended to Applicants' representative, Christopher Ward, during the personal interview conducted on October 10, 2000.

In the outstanding Official Action, the drawings were objected to for the reasons stated on page 2 of the outstanding Official Action. The last paragraph on page 1 has been amended to clarify that Figures 11 and 12 depict circuit board examples of the prior art. Submitted concurrently herewith is a Letter Requesting Approval of Drawing Changes which

includes amendments in red ink to Figures 11 and 12 that add the legend "Prior Art." Additionally, amendments have been made to Figures 2, 3, and 12 to correct any cross-hatching problems, as discussed during the interview. Note, however, that the cross-hatching used in the figures is merely representative of preferred embodiments of the present invention, and are not meant to limit the scope of the claims in any manner. As discussed during the interview, the objection to Figure 11 based upon cross-hatching problems was in error and should have been directed to the cross-hatching in Figure 12. Accordingly, Figure 12 has been amended to address the cross-hatching problem with respect to element 23. Accordingly, the Applicants request the withdrawal of the objections to the drawings.

Claims 7-9 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The specific grounds for rejection are recited on page 3 of the Official Action. Claims 7 and 9 have been amended to remove the rejected language therefrom, specifically the phrase "configured to extend" and the phrase "configured to correspond to the plurality of bumps." Accordingly, the Applicants request the withdrawal of the indefiniteness rejections.

Claim 7 was rejected under 35 U.S.C. 102(b) as being anticipated by Martin (U.S. Patent No. 3,908,185). Claims 7-9 were rejected under 35 U.S.C. 102(e) as being anticipated by Lebaschi (U.S. Patent No. 5,764,485). For the reasons set forth below, the Applicants respectfully request the withdrawal of the anticipation rejections.

Claim 7 has been amended to include the subject matter of Claim 8. Additionally, Claim 9 has been rewritten in independent form. Accordingly, the Applicants submit that the rejections based upon the Martin patent should be withdrawn.

Claims 7 and 9 of the present application recite a circuit board comprising a main body, and a conductive layer provided on the main body. The conductive layer is defined as having a conductive pattern having at least one bonding area. The conductive layer is further defined as having at least one of an isolated notch part and a recess located proximate to and not extending within the at least one bonding area.

The Lebaschi patent a multi-layer PCB blockade via-pad connection. Figure 10 depicts two alternate circular via-pad shapes (29 and 29'), with one pad having a straight formed crisscross-relief (non-conductive open-space region)(40) bisecting the via-hole (30) and the other pad having a fanned shape (40') bisecting via-hole (30). As depicted in, for example, Figure 7, the via-pad (29) represents the bonding area for the solder-ball (13).

The Applicants submit that the Lebaschi patent does not disclose or suggest all of the elements of Claims 7 and 9. For example, the Lebaschi patent does not teach or suggest a circuit board having a conductive layer having at least one of an isolated notch part and a recess located proximate to and not extending within at least one bonding area. The Official Action cites the Lebaschi patent for the teaching of a bonding area (29) and an isolated notch (40'). As clearly depicted in Figure 10 of the Lebaschi patent, the structure (40') is within the bonding area (29), which is in direct contradiction to the express language of Claims 7 and 9. Accordingly, the Applicants respectfully submit that the circuit boards recited in Claims 7 and 9 of the present application are distinguishable over the Lebaschi patent, and therefore the Applicants request the withdrawal of the anticipation rejection based upon the Lebaschi patent.

Newly added Claims 13-15 are considered allowable as they recite features of the invention that are neither disclosed, taught, nor suggested by the references of record.

Consequently, in view of the above discussion, it is respectfully submitted that Claims 7, 9, and 13-15 are patentably distinguishing over the cited art. The present application is therefore believed to be in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully submitted,

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